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AD102/AD104- SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$ and power supply of $\pm 15\text{ V} \pm 5\%$ unless otherwise noted)

| Parameter | Min | Typ | Max | Unit | Notes |
|--|--------|------------------|-------------|----------|---|
| ACCURACY | | | | | |
| Gain Range | 1 | | 100 | V/V | |
| Unity Gain Error | | ±0.5 | ±5.0 | % | |
| vs. Temperature | | ±45 | | ppm/°C | ±100 ppm/°C max |
| vs. Time | | ±50 | | ppm | Per √1,000 Hours |
| vs. Supply Voltage, AD102 ¹ | | ±0.01 | | %/V | |
| vs. Supply Voltage, AD104 ¹ | | ±0.001 | | %/V | |
| Nonlinearity ² | | | ±0.05 | % | |
| INPUT VOLTAGE RATINGS | | | | | |
| Linear Differential Range | ±5.0 | | | V | Between IN + and IN - |
| CMV, Input to Output ² | | | | | |
| AC, 60 Hz, Sinusoidal Waveform | 500 | | | V rms | 100% Tested |
| DC | | 700 | | V pk-pk | |
| Common-Mode Rejection (CMR) | | | | | |
| RS ≤ 100 Ω, AD102 ¹ | | 100 | | dB | |
| RS ≤ 100 Ω, AD104 ¹ | | 105 | | dB | |
| RS ≤ 1 kΩ, AD102 ¹ | | 95 | | dB | |
| RS ≤ 1 kΩ, AD104 ¹ | | 105 | | dB | |
| Leakage Current | | 0.5 | | μA | 2 μA max, In to Out, 240 V rms @ 60 Hz |
| INPUT CHARACTERISTICS | | | | | |
| Input Offset Voltage, Initial | | | (±15 ±15/G) | mV | +25°C |
| vs. Temperature | | (±10 ±10/G) | | μV/°C | 0°C to +70°C |
| Input Bias Current, Initial | | ±100 | | pA | +25°C |
| vs. Temperature | | ±20 | | nA | 0°C to +70°C |
| Input Difference Current, Initial | | ±10 | | pA | +25°C |
| vs. Temperature | | ±2 | | nA | 0°C to +70°C |
| Input Voltage Noise | | | | | |
| 0.1 Hz to 100 Hz | | 4 | | μV pk-pk | |
| f > 200 Hz | | 50 | | nV/√Hz | |
| Differential Input Impedance | | 10 ¹² | | Ω | |
| Common-Mode Input Impedance | | 2G 5.5 | | Ω pF | |
| FREQUENCY RESPONSE | | | | | |
| Bandwidth, Full Power (-3 dB) | | | | | |
| AD102 ¹ | | 1.5 | | kH z | VIN ≤ ±5 V, G = 1-50 V/V |
| AD104 ¹ | | 4.0 | | kH z | VIN ≤ ±5 V, G = 1-50 V/V |
| Settling Time | | 1.0 | | ms | Time to ±10 mV from 10 V Step Input |
| RATED OUTPUT | | | | | |
| Output Voltage Range | | | | | |
| Between OUT HI and OUT LO | ±5.0 | | | V | |
| Between OUT HI or LO to PWR/CLK COM | | ±6.5 | | V | |
| Output Resistance | | | | | |
| AD102 ¹ | | 8 | | kΩ | |
| AD104 ¹ | | 4 | | kΩ | |
| Output Ripple | | | | | |
| 100 kH z Bandwidth | | 10 | | mV pk-pk | |
| 5 kH z Bandwidth | | 0.5 | | mV rms | |
| POWER SUPPLY (AD102 ONLY) ¹ | | | | | |
| Supply Voltage | | | | | |
| Rated Performance | +14.25 | +15 | +15.75 | V dc | |
| Operational Performance | +13.5 | +15 | +16.5 | V dc | |
| Supply Current | | 5 | | mA | |

| Parameter | Min | Typ | Max | Unit | Notes |
|--|-------|-----|--------------------------------|--------------|--|
| CLOCK OSCILLATOR (AD104 ONLY) ¹ | | | | | |
| Source Voltage Amplitude | 14.25 | 15 | 15.75 | V pk-pk | ±7.5 V Amplitude Within ±15 V Range |
| Square Wave Frequency | | 25 | | kHz | ±5 kHz |
| Duty Cycle | | 50 | | % Hi vs. Low | ±2% |
| TEMPERATURE RANGE | | | | | |
| Rated Performance | 0 | | +70 | °C | |
| Operating | -40 | | +85 | °C | |
| Storage | -40 | | +85 | °C | |
| PACKAGE DIMENSIONS | | | | | |
| SIP Style Package (Y) | | | 2.08 × 0.260 × 0.625 in. (max) | | Not Including Pin Length |

NOTES

¹Specification(s) apply to one model only, either AD102 or AD104, as indicated.

²Nonlinearity is specified as a % deviation from a best fit straight line.

³All units 100% tested by "Partial Discharge" method @ 750 V rms for 5 sec, 150 pc maximum allowable discharge.

Specifications subject to change without notice.

PIN DESIGNATIONS

| Pin | Function |
|-----|---------------------|
| 1 | OUT HI |
| 2 | PWR/CLK COM |
| 3 | FB |
| 4 | ICOM |
| 5 | IN + |
| 6 | IN - |
| 7 | +15 V DC (AD102) |
| 8 | CLOCK INPUT (AD104) |
| 9 | OUT LO |

ORDERING GUIDE

| Model | Package | Max CMV | Nonlinearity |
|---------|-----------|-----------|--------------|
| AD102JY | SIP Style | 500 V rms | 0.05% |
| AD104JY | SIP Style | 500 V rms | 0.05% |

DIFFERENCES BETWEEN THE AD102 AND AD104

The primary difference between the AD102 and AD104 is that the AD102 contains an integral clock oscillator circuit and the AD104 does not. As a result, the AD102 operates when supplied +15 V dc power while the AD104 requires power in the form of 15 V, 25 kHz square wave source. Typically a clock source for an AD104 will drive multiple devices to reduce the per channel cost of the source and to provide perfect oscillator synchronization between devices. The AD104 also consumes slightly less power and has more than twice the bandwidth of the AD102.

In situations where only one or a few isolators are used, the convenience of stand-alone operation offered by the AD102 may provide a greater user advantage than use of the AD104. For maximum product flexibility both the AD102 and AD104 can be accommodated by using a single universal layout for device interchangeability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD102/AD104

INSIDE THE AD102 AND AD104

The AD102 and AD104 use an amplitude modulation technique to exploit transmission of low frequency signal levels through an isolation barrier produced by a signal transformer including signals at a dc level (Figures 1 and 2). Additionally a separate transformer is incorporated to provide power to the isolated input port of the device. It is driven by a 25 kHz, 15 V amplitude square wave generated internally by the AD102, supplied externally for the AD104.

The device outputs are not buffered so the user may interchange output leads for signal inversion. In multichannel applications the outputs can be multiplexed with a single buffer following the multiplexer to minimize offset errors while reducing power consumption and cost.

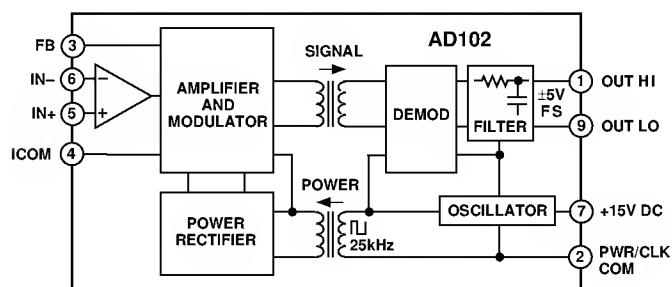


Figure 1. AD102 Functional Block Diagram

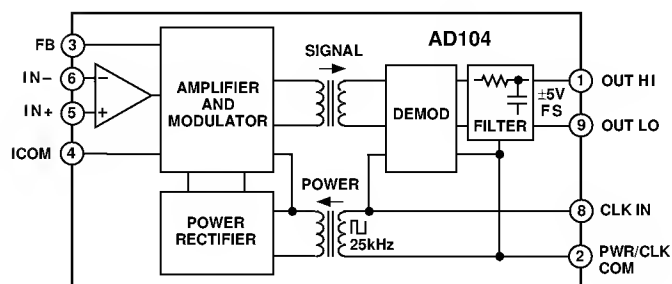


Figure 2. AD104 Functional Block Diagram

USING THE AD102 AND AD104

Powering the AD102

The AD102 requires only a single +15 V DC power supply connected as shown in Figure 3 to operate. A series 1.3 k Ω resistor and 1.0 μ F capacitor are connected across the +15 V DC and COMMON pins to aid in filtering power line variations.

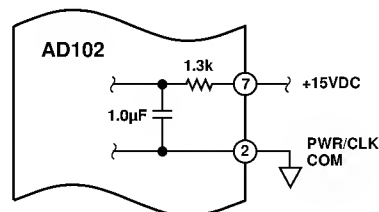


Figure 3. AD102 Power Input

Powering the AD104

The AD104 requires its power in the form of a 15 V p-p, 25 kHz square wave from an external source as shown in Figure 4 (NOTE: pinout for AD246 clock driver shown).

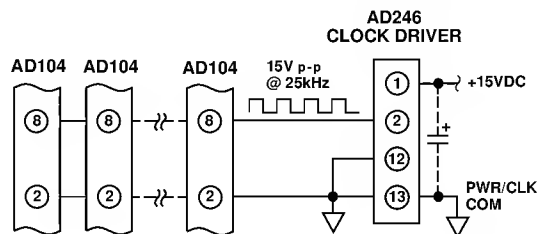


Figure 4. Typical Multiple AD104 Connection

AD104 Clock Source

The AD246 clock driver designed to power the AD204 is a clock driver that can be used to supply the required clock for the AD104 from a +15 V DC supply (refer to the AD202/AD204 data sheet for AD246 specifications).

For designs where the lowest cost per channel approach is desired, it is usually more cost efficient for designers to consider a discrete onboard clock source such as the circuit shown in Figure 5 (essentially an AD246).

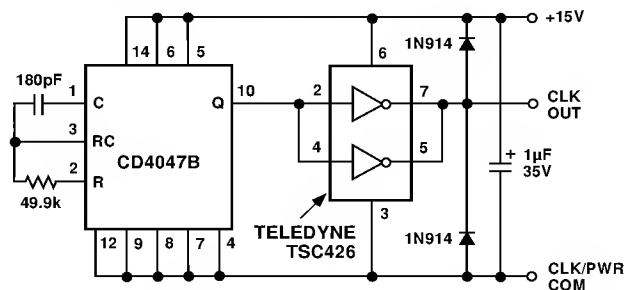


Figure 5. Typical Clock Driver Circuit

Although this circuit generates a unipolar clock output of 0 V–15 V, any 15 V amplitude square wave at 25 kHz with a duty cycle of 50% is acceptable. This is possible since the AD104 clock input is ac coupled by means of a 0.1 μ F capacitor as shown in Figure 6. The source, therefore, only needs to be ± 7.5 V p-p in total amplitude and may be offset as desired. A recommended maximum amplitude limit of ± 15 V with respect to PWR/CLK COM should not be exceeded.

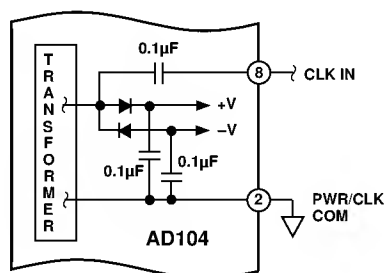


Figure 6. AD104 Clock Input

One clock circuit will usually drive multiple AD104s (typically 4, 8 or 16 units). If many AD104s are to be operated from a single source, external bypass capacitors should be used with a value of at least 1 μ F for every five isolators used. Place the capacitor as close as possible to the clock driver.

Input Configuration

The AD102 and AD104 are very easy to use in a wide range of applications. The input stage connections (IN+, IN–, FB, ICOM) approximate a “vanilla” type op amp input and may for all intents and purposes be treated as such. Most any typical circuit connection that is valid for a standard op amp can be accommodated, so long as it is expected to perform within the specifications herein (i.e., limited gain and bandwidth parameters).

Figure 7 shows the most common input configuration, which is unity gain operation. This configuration is appropriate where the input signal is within the range of ± 5 V or where larger signals have been previously attenuated, usually by means of a traditional resistor divider technique.

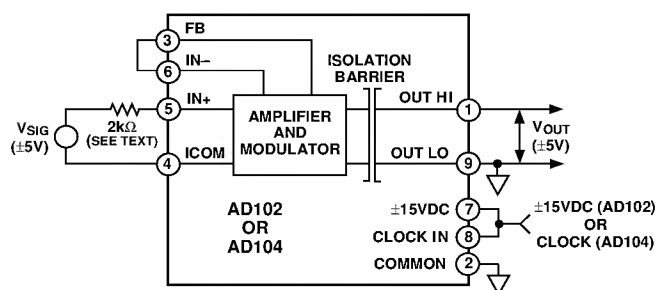


Figure 7. Unity Gain Application

For gains larger than unity, the addition of a gain and feedback resistor allows amplification of smaller signals up to a higher level. Whenever practical, any low level signal should be amplified to meet a full ± 5 V output swing. This helps reduce the effective output ripple contribution introduced to the original signal during modulation, isolation and subsequent filtering as seen at the output.

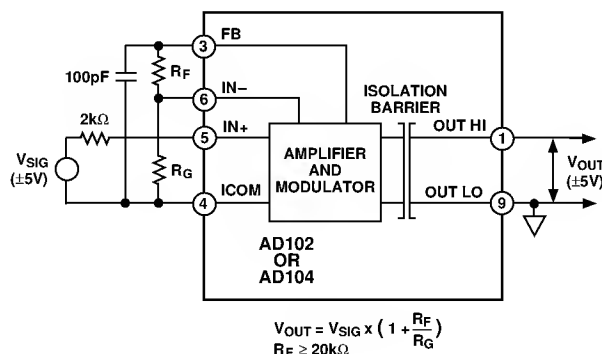


Figure 8. Input Connection for Gain > 1

When taking a gain of more than 5 V/V, addition of a 100 pF capacitor is recommended; it is not needed at lower gains, but if used will not adversely affect operation. Additionally, whenever the isolation amplifier is not powered, a negative input voltage of approximately 2 V may cause an input current to flow. If the signal source can supply more than a few mA of current, a 2 k Ω limiting resistor in series with IN+ is recommended. This is especially advised when using AD102s as they may not power up properly with a high input current present, (see Figures 7 and 8 for examples).

Synchronization

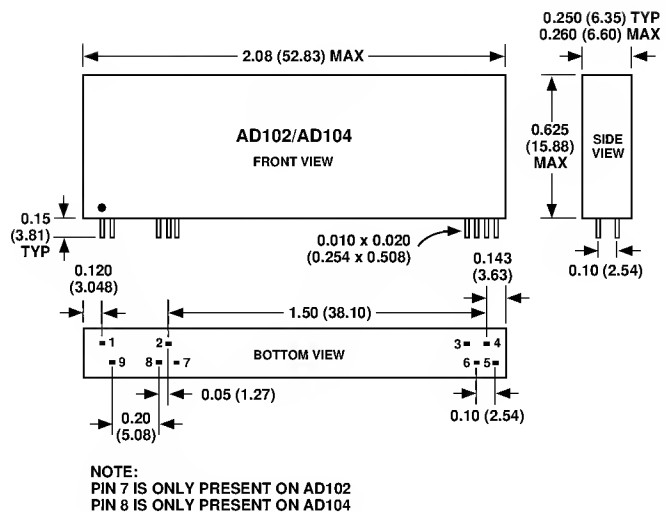
Since the AD104 operates from a common clock, synchronization is inherent. AD102s will normally not interact to produce beat frequencies even when mounted on 0.3 inch centers. Interaction may occur in very rare situations where a large number of long, unshielded input cables are bundled together. In such cases, shielded cable may be required or AD104s can be used.

For related information and application examples refer to the AD202/AD204 and AD210 data sheets.

AD102/AD104

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



C1954-10-10/94

PRINTED IN U.S.A.